

FML60N105E7
N-Channel ϵ MOS E7 Power MOSFET
600 V, 31 A, 105 m Ω



Description

The 600V ϵ MOS E7 is an advanced Faster Semiconductor's Super Junction MOSFET family by utilizing charge balance technology for excellent low on-resistance and gate charge. This technology combines the benefits of a fast switching performance with ease of usage and robustness. Consequently, the ϵ MOS E7 family is suitable for application requiring high power density and superior efficiency. PQFN88 Kelvin source configuration package offers excellent switching performance thanks to separated power and drive sources for high efficiency and high switching frequency applications.

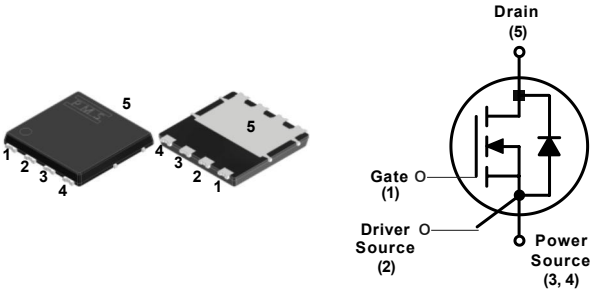
Applications

- PFC, Hard & Soft Switching Topologies
- Industrial & Consumer Power Supplies

Features

$BV_{DSS} @ T_{J,max}$	I_D	$R_{DS(on),max}$	$Q_{g,typ}$
650 V	31 A	105 m Ω	52 nC

- Reduced Switching & Conduction Losses
- Lower Gate Resistance
- 100% Avalanche Tested
- Pb-free, Halogen Free, RoHS and MSL2a Compliant



Absolute Maximum Ratings ($T_C = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate to Source Voltage	± 30	V
I_D	Drain Current	Continuous ($T_C = 25^{\circ}C$)	A
		Continuous ($T_C = 100^{\circ}C$)	
I_{DM}	Drain Current	Pulsed (Note1)	A
E_{AS}	Single Pulsed Avalanche Energy	(Note2)	mJ
I_{AS}	Avalanche Current	(Note2)	A
E_{AR}	Repetitive Avalanche Energy	(Note1)	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt	(Note3)	
P_D	Power Dissipation	($T_C = 25^{\circ}C$)	W
		Derate Above $25^{\circ}C$	W/ $^{\circ}C$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^{\circ}C$
T_L	Maximum Lead Temperature for Soldering	260	$^{\circ}C$

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.48	$^{\circ}C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note4)	45	

Package Marking and Ordering Information

Part Number	Top Marking	Package	Packing Method	Quantity
FML60N105E7	FML60N105E7	PQFN88	Tape & Reel	3000 units

Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	600			V
		$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 150^\circ\text{C}$	650			
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$		2.1		
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 2.1\text{ mA}$	2.5		4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 11.5\text{ A}$		89	105	m Ω

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V},$ $f = 250\text{ kHz}$		2270		pF
C_{oss}	Output Capacitance			58		pF
$C_{o(tr)}$	Time Related Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$		670		pF
$C_{o(er)}$	Energy Related Output Capacitance			92		pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DS} = 400\text{ V}, I_D = 15.3\text{ A},$ $V_{GS} = 10\text{ V}$		52		nC
Q_{gs}	Gate to Source Charge			12.7		nC
Q_{gd}	Gate to Drain "Miller" Charge			22.4		nC
R_G	Gate Resistance	$f = 1\text{ MHz}$		0.9		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 400\text{ V}, I_D = 15.3\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 10\text{ }\Omega$ See Figure 13		18		ns
t_r	Turn-On Rise Time			9		ns
$t_{d(off)}$	Turn-Off Delay Time			83		ns
t_f	Turn-Off Fall Time			7		ns

Source-Drain Diode Characteristics

I_S	Maximum Continuous Diode Forward Current			31	A
I_{SM}	Maximum Pulsed Diode Forward Current			93	A
V_{SD}	Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 15.3\text{ A}$		1.2	V
t_{rr}	Reverse Recovery Time	$V_{DD} = 400\text{ V}, I_{SD} = 15.3\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$		346	ns
Q_{rr}	Reverse Recovery Charge			5.1	μC

※Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{AS} = 5.6\text{ A}, R_G = 25\text{ }\Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 15.3\text{ A}, di/dt \leq 100\text{ A}/\mu\text{s}, V_{DD} \leq 400\text{ V}$, starting $T_J = 25^\circ\text{C}$.
4. Device on 1.0 x 1.0 inch and 2-oz copper pad on 1.5 x 1.5 inch PCB FR4.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

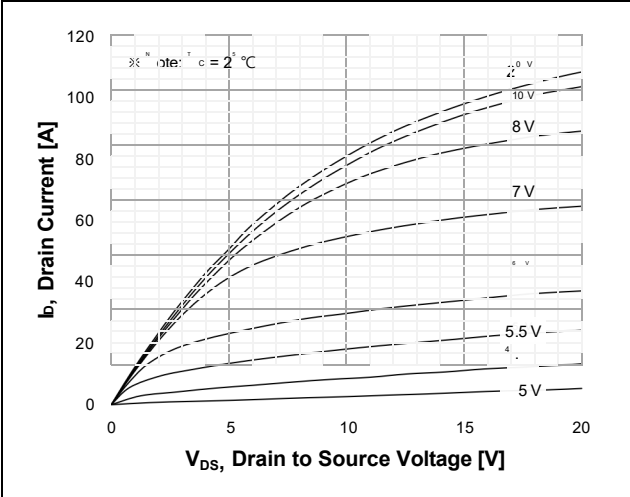


Figure 2. Transfer Characteristics

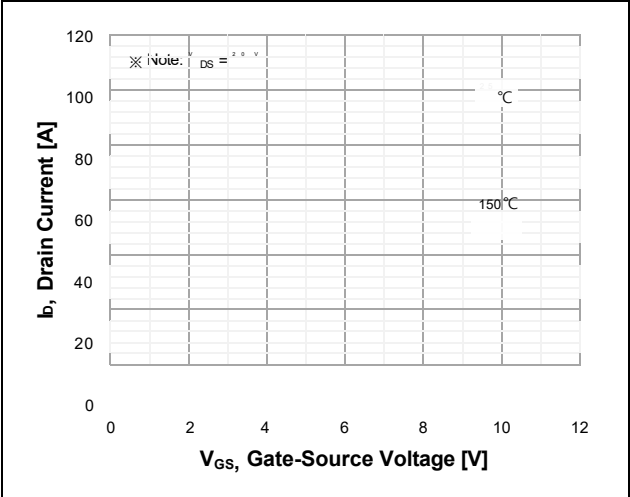


Figure 3. On-Resistance Characteristics vs. Drain Current and Gate Voltage

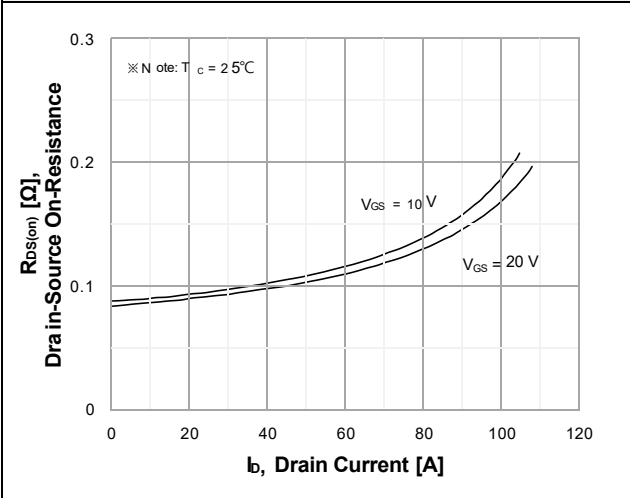


Figure 4. Diode Forward Voltage Characteristics vs. Source-Drain Current and Temperature

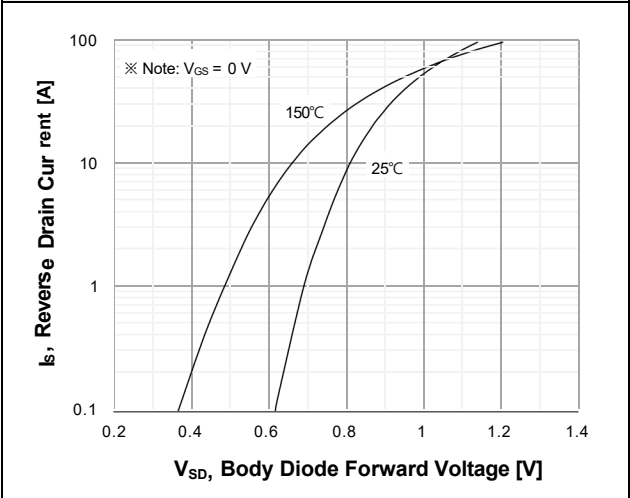


Figure 5. Capacitance Characteristics

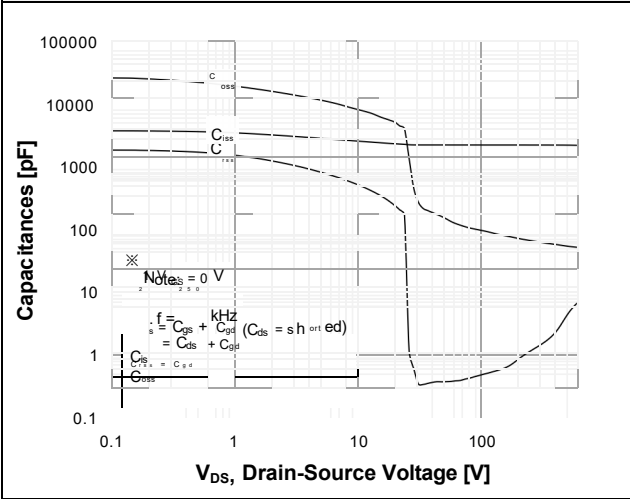
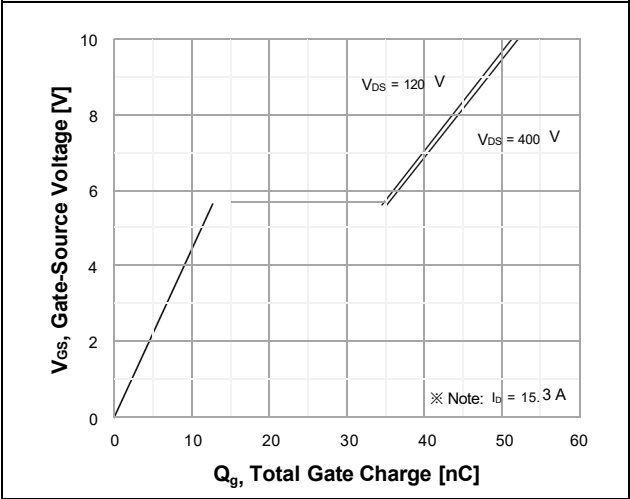


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics

Figure 7. Breakdown Voltage Characteristics vs. Temperature

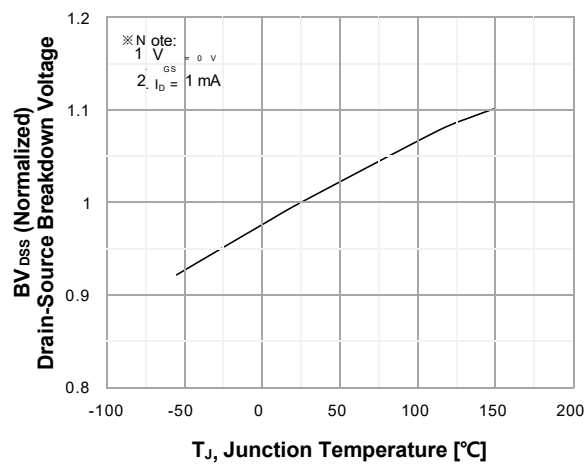


Figure 8. On-Resistance Characteristics vs. Temperature

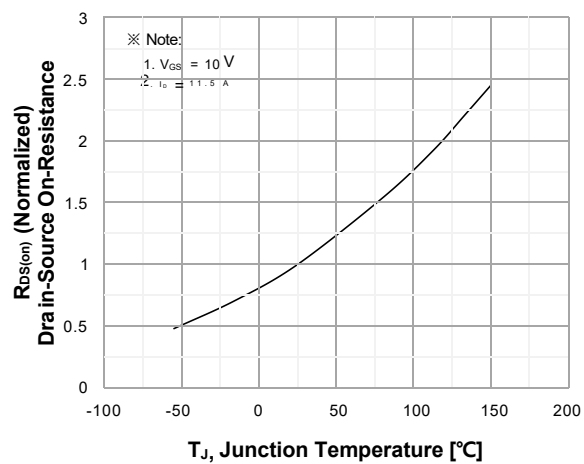


Figure 9. Maximum Safe Operating Area

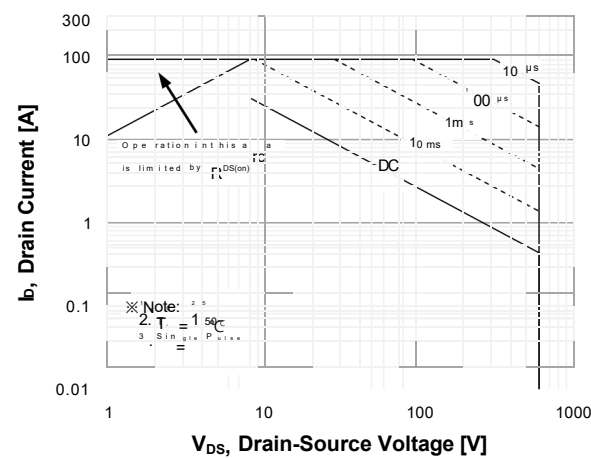


Figure 10. Maximum Drain Current vs. Case Temperature

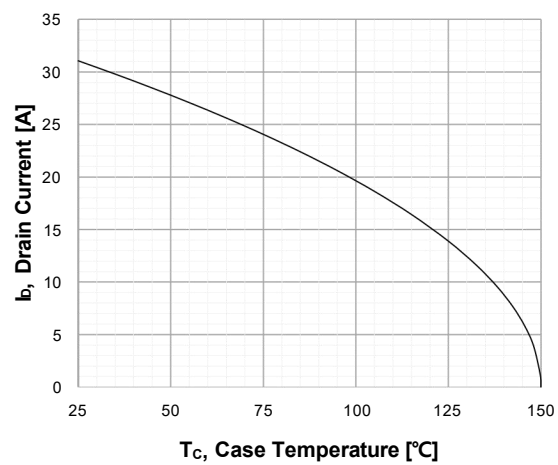


Figure 11. E_{OSS} vs. Drain to Source Voltage

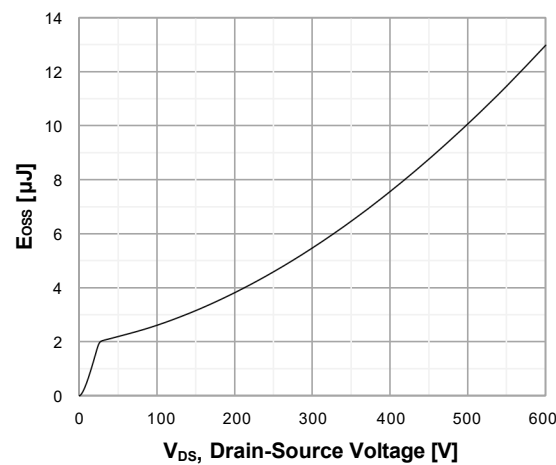
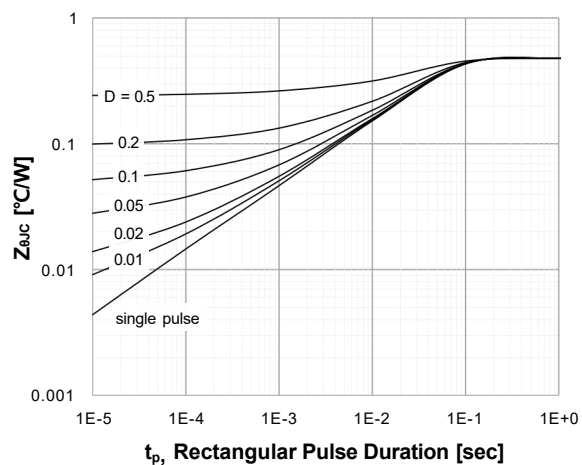


Figure 12. Transient Thermal Response Curve



Test Circuits

Figure 13. Inductive Load Switching Test Circuit and Waveforms

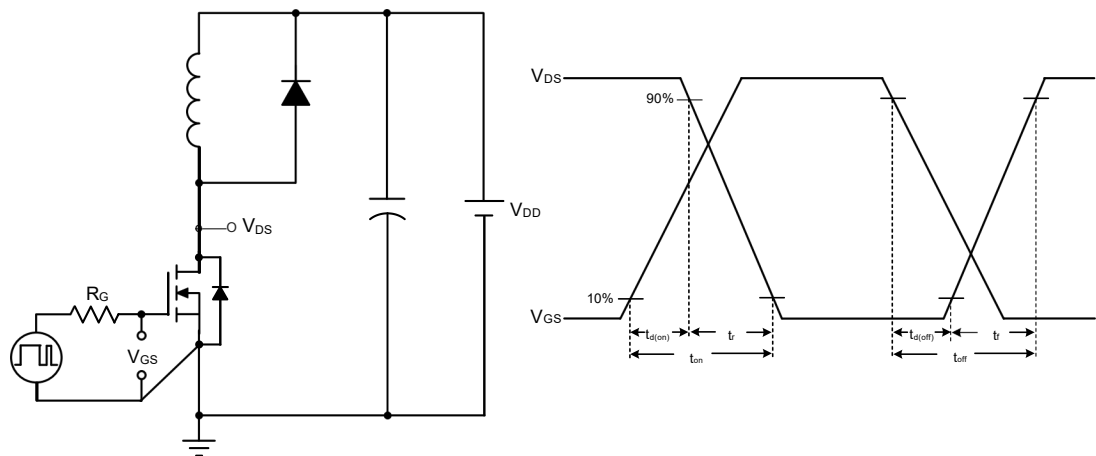


Figure 14. Unclamped Inductive Switching Test Circuit and Waveforms

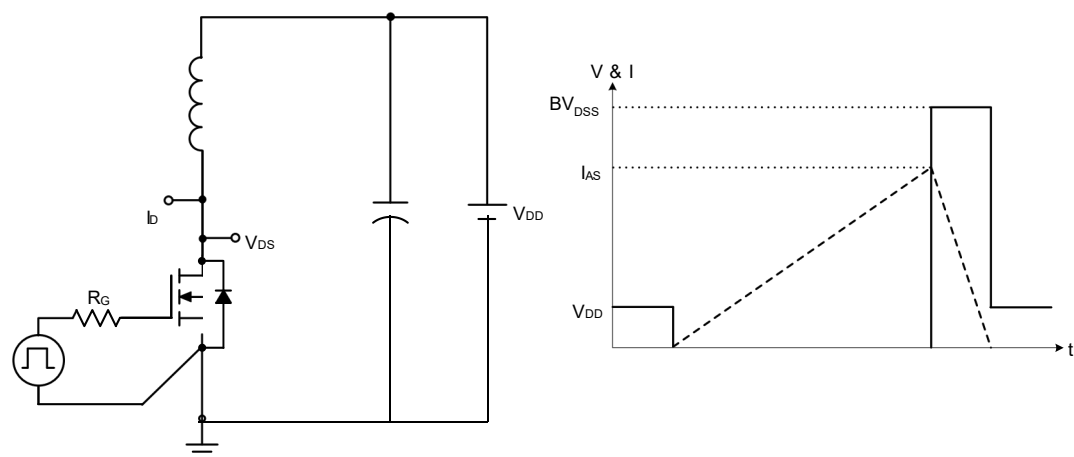
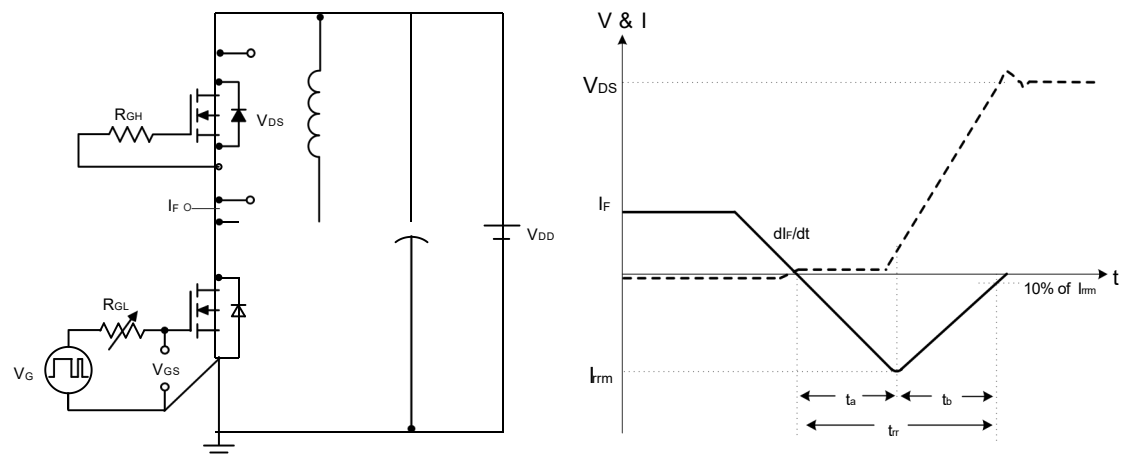
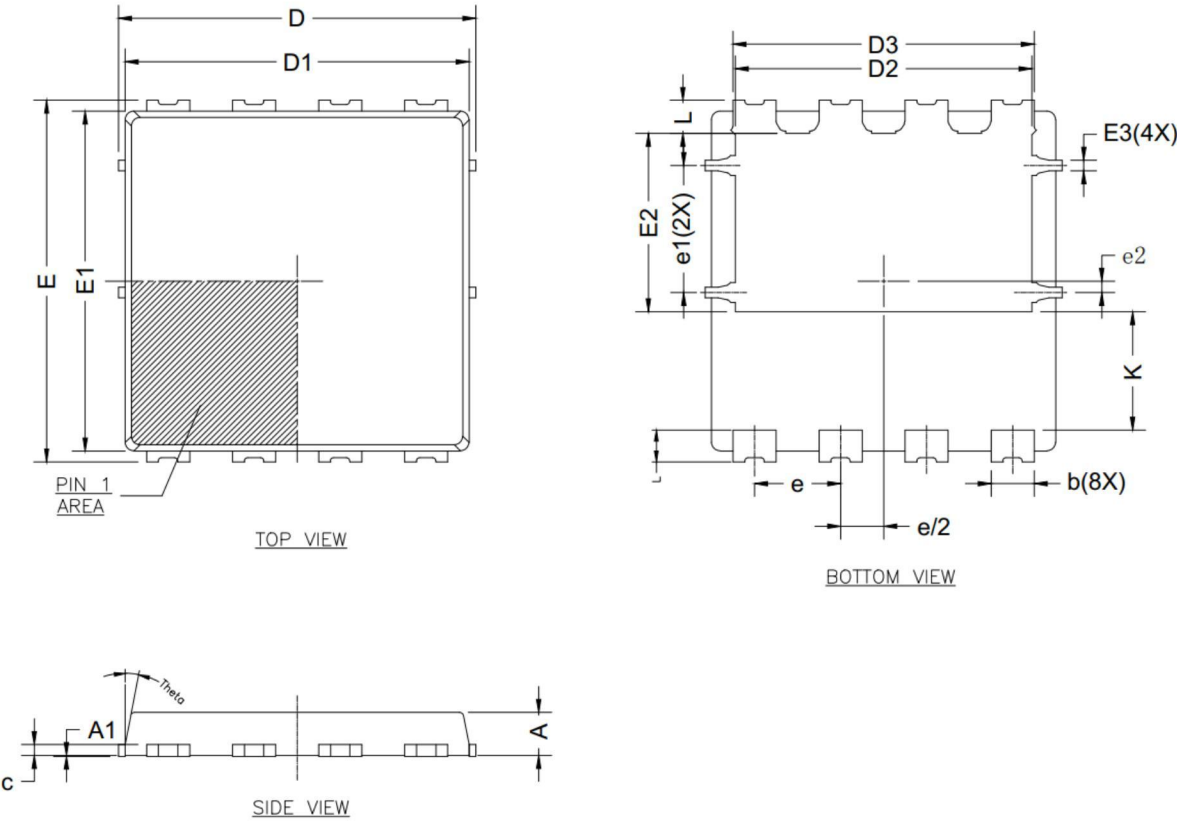


Figure 15. Peak Diode Recovery dv/dt Test Circuit and Waveforms



Package Outlines

PQFN88



SYM BOL	Common		
	DIMENSIONS MILLIMETER		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.90	1.00	1.10
c	0.20	0.25	0.30
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	4.0450	4.145	4.245
E3	0.15	0.25	0.35
e	2.00 BSC.		
e/2	1.00 BSC.		
e1	2.95 BSC.		
e2	0.265 BSC.		
K	2.68	2.75	2.82
L	0.67	0.77	0.87
L1	0.64	0.74	0.84
θ	0°	-	12°